CMOS NAND Gate

The below figure shows the figure of CMOS as NAND gate. It consists of two series NMOS transistors between Y and ground and two parallel PMOS transistors between Y and VDD as shown below

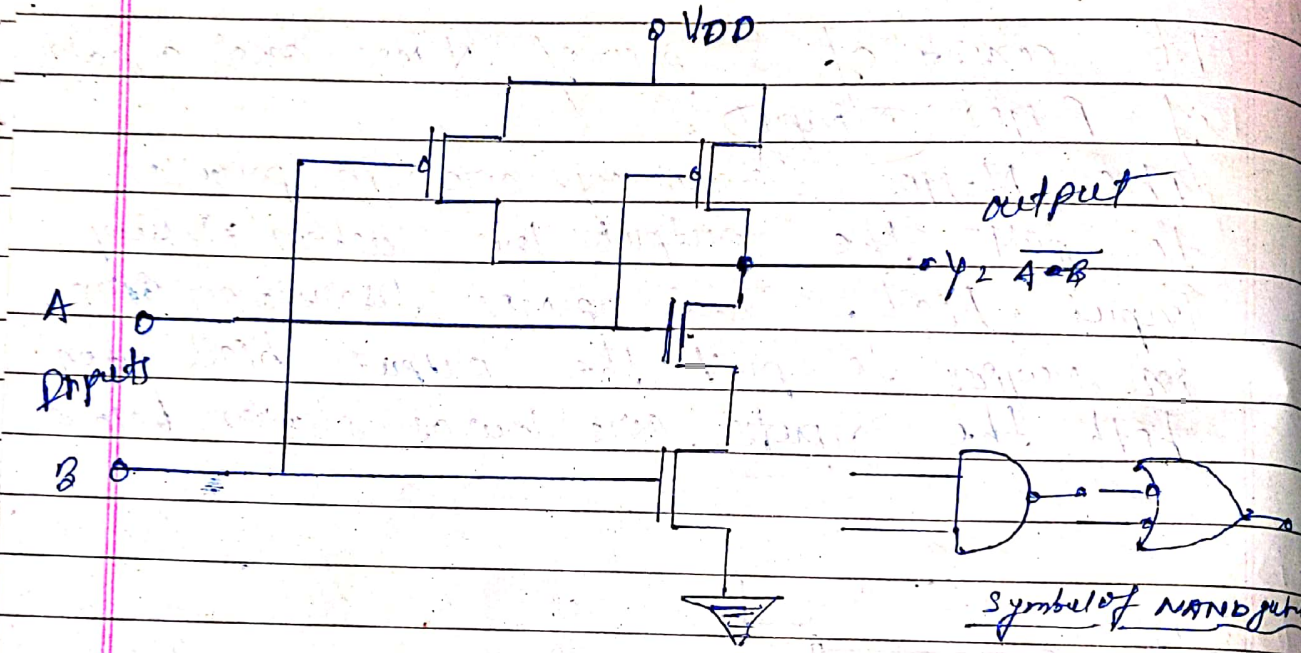

Fig: CMOS as NAND gate

Operation:

1) If either input A or B is logic 0, at least one of the two NMOS transistors will be turned off breaking the path from Y to ground. But at least one of the PMOS transistors will be ON creating a path from Y to VDD.
2) Hence the output Y will be high.
3) If both the inputs are high both of the N-MOS transistors will be ON. Hence the output would be ~~ON~~ of logic low i.e 0V.